THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAMES A. WILSON, JR.,
ANTHONY C. MILLER ,
MICHAEL W. RHODEHAMEL,
ADRIAN CARBINE, DEREK B.I. FELTHAM,
and SUMEET AGRAWAL

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Appeal No.1997-3134
Application 08/434,163[1]

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ON BRIEF

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Before THOMAS, FLEMING, and DIXON, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This a decision on appeal from the final rejection of claims 1 through 6, 15 through 17 and 19, all of the claims pending in the present application. Claims 7 through 14, 18 and 20 have been

[1] Application for patent filed May 2, 1995.

canceled.

The invention relates to the field of microprocessors and more particularly to a technique of providing internal access to the microprocessor through a standardized test access port.

On page 5 of the specification, Appellants disclose that external access to internal low level structures of a microprocessor allows for flexibility in performing diagnostics on a microprocessor which ultimately reduces time required to test and debug the microprocessor.

On pages 9 and 10 of the specification, Appellants disclose that figure 1 shows an access test port unit 11. On page 11 of the specification, Appellants disclose that the test access port unit 11 is coupled to a control register unit 13. Appellants further disclose that control register unit 13 is coupled to control buses 15 and 16 to allow access to control registers 14 of the microprocessor 10. Appellants disclose on page 12 that the circuit shown in figure 1 allows data to be written into the control registers of the microprocessor or read from the control register microprocessor through a serial port provided into the test access port unit 11.

Independent claim 1 is reproduced as follows:

1. A microprocessor providing external diagnostic access comprising:

a plurality of control registers;

an internal bus coupled to said control registers;

a test access port (TAP) configured to receive external programming signals in a serial format;

said TAP including a first register that receives a first instruction command in said serial format and converts said first instruction command to a parallel format;

a control register unit that receives, in said serial format, an address to one of said control registers for data access thereto, said control register unit being coupled to said TAP and said internal bus;

said control register unit including a second register that converts data received in said serial format to said parallel format;

in a write operation, said control register unit causing data to be transferred from said second register to said one of said control registers specified by said address responsive to said first instruction command;

in a read operation, said control register unit causing data to be transferred from said one of said control registers to said second register responsive to said first instruction command.

The Examiner relies on the following references:

Swoboda et al. (Swoboda)	5,329,471	July 12, 1994
Andrews	5,459,737	Oct. 17, 1995

Claims 1 through 6, 15 through 17 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Andrews in view of Swoboda.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 6, 15 through 17 and 19 under 35 U.S.C. § 103.

The Examiner has failed to set forth a **prima facie** case of obviousness. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

Appellants argue on pages 8 and 9 of the brief that Andrews teaches away from using a test access port (TAP) for functional testing. Appellants point out that Andrews teaches a built-in current monitor for sensing and measuring static current in CMOS and MOS circuit modules of IC devices. Appellants point out that Andrews teaches that static current testing is preferable to traditional logical function testing in column 1, lines 16 through 34 and column 1, line 54 through column 2, line 3. Appellants point out that Andrews specifically states in the background section that "static current testing provides substantially greater accuracy than traditional logical testing by voltage measurements, sometimes referred to as 'stuck at fault' testing or functional testing." Appellants cited column 1, lines 30 through 34. Appellants argue that this is a teaching away from the invention claimed by the Appellants and that the Appellants' present invention, contrary to the teachings of Andrews, claims the use of the TAP for functional testing.

On page 12 of the brief, Appellants argue that neither nor Swoboda teach reading from or writing to control registers in the microprocessor. Appellants point out that Appellants' independent claim 1 recites "in a write operation, said control register unit causing data to be transferred from said

second register to said one of said control registers specified by said address responsive to said first instruction command; in a read operation, said control register unit causing data to be transferred from said one of said control registers to said second register responsive to said first instruction command." We note that independent claim 15 recites similar language. Appellants argue that Andrews does not read from or write to any component outside of the TAP or the TAP's internal TDRs. Appellants further pointed out that Swoboda does not teach accessing control registers for reading or writing either.

In response to Appellants' argument that Andrews teaches away from the claimed invention, the Examiner responds on page 8 of the Examiner's answer stating that Andrews does teach a TAP having registers BICSC and ITV TDR for testing. The Examiner further argues that these registers are not excluded from the inclusion of the use of TAP for functional testing. In response to Appellants' argument that the references do not teach reading from or writing to the control register, the Examiner responds by arguing that although Andrews does not explicitly teach reading from or writing to the control register, Andrews does suggest that boundary scan registers BSR apply a test vector at selected input or nodes of the CMOS modules during a test mode. The Examiner argues that it would been obvious to one of ordinary skill art in the art to realize that the features of writing to and reading from the CMOS modules are encompassed during applying test vector to the CMOS modules during testing.

We note that our reviewing court states that "when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc***., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), **cert. denied**, 519 U.S. 822 (1996), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc***., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984). In addition, our reviewing court reasons in ***Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc***., 73 F.3d 1085, 1088-89, 37 USPQ2d 1237, 1239-40 (Fed. Cir. 1995), **cert. denied**, 519 U.S. 822 (1996), that for the determination of obviousness, the court must answer whether one of ordinary skill in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Appellants.

We agree with the Appellants that Andrews would have reasonably led those skilled in the art away from the solution of reading in and reading out diagnostic instructions to the microprocessor as claimed by Appellants to a solution of using a static current through the CMOS or MOS circuit. Andrews teaches in column 1, lines 25 through 30, that testing using static current through the CMOS or MOS provides substantially greater accuracy and traditional logic testing. Andrews further teaches in column 5, lines 29 through 45, that the object of the invention is to provide a built-in current monitor for sensing and measuring static current in CMOS and MOS circuits. When reading the Andrews reference as a whole, we fail to find any teaching that would lead one of ordinary skill in the art to

provide a write operation or a read operation to read in diagnostic instructions into a microprocessor. Upon a careful review of Swoboda, we find that Swoboda teaches an emulation device including a serial scan testing interface. We find that Swoboda fails to teach or suggest a write operation or a read operation causing data to be read into or written out of control registers of a microprocessor for diagnostic testing.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992) ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Upon our review of Andrews and Swoboda we find that the references fail to suggest any desirability of modifying the Andrews static current testing device to provide a microprocessor having external diagnostic access by having a read operation and a write operation in which the control registers of the microprocessor art can be accessed externally as recited in Appellants' claims.

In view of the forgoing, we have not sustained the rejection of claims 1through 6, 15 through 17 and 19 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS	)
Administrative Patent Judge	)
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	)
	) BOARD OF PATENT
MICHAEL R. FLEMING	)
Administrative Patent Judge	) APPEALS AND
	)
	) INTERFERENCES
	)
JOSEPH L. DIXON	)
Administrative Patent Judge	)

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